Revised Format for Amendments promulgated earlier in 2003 by the U.S. Patent and Trademark Office.

As the three-month shortened statutory period for reply is due October 27, 2005, this Response is therefore considered timely filed.

AMENDMENTS

In the Specification

Please amend the specification paragraph [0021] at page 6, line 15 to page 7, line 17 as indicated below.

Please amend the Abstract at page 15 as indicated below.

Applicant respectfully submits that no new matter has been added to the specification and abstract. Applicant respectfully requests that the amendments shown herein below be accepted and entered into the file of the above styled case.

In the Claims

Please cancel claims 16, 26 and 28 without prejudice to file same in a continuation, continuation-in-part, divisional or co-pending application, and amend the remaining claims as indicated below.

Applicant respectfully submits that no amendments have been made to the pending claims for the purpose of overcoming any prior art rejections that would restrict the literal scope of the claims or equivalents thereof.

AMENDMENT TO THE SPECIFICATION SHOWING AMENDMENTS MADE THERETO

[0021] The ESD-protection structure of Figure 1, generally represented by the numeral 100, is located substantially under an integrated circuit bond pad 114. The ESD-protection structure 100 comprises alternating P+ diffusions 126 and N+ diffusions 128, located substantially under the integrated circuit bond pad 114. The P+ diffusions 126, may be arranged in stripes (see Figure 1b) or in alternating squares (see Figure 1c), and are connected to the bond pad 114 with conductive vias 116 through an insulating layer 124 located between the bond pad 114 and the P+ diffusions 126 and the N+ diffusions 128. The N+ diffusions 128 are adjacent to and surround the P+ diffusions 126. Other shapes for the P+ diffusions 126 may be used and are contemplated herein. An N+ diffusion 128a surrounds the N+ diffusions 128 and P+ diffusions 126, and ties together the N+ diffusions 128 so as to form a continuous N+ diffusion 128 completely around each of the P+ diffusions 126. The N+ diffusions 128 may be formed as one N+ diffusion 128 during fabrication of the integrated circuit. The N+ diffusions 128 are insulated from the bond pad metal by the insulating layer 124. The P+ diffusions 126 are connected to the bond pad 114 by conductive vias 116. An N- well 130 is located substantially under the N+ diffusions 128 and the P+ diffusions 126. The surrounding N+ diffusion 128a partially overlaps the edge of the N- well 130 below. ~~The integrated circuit substrate 132 comprises P- semiconductor material that behaves as a~~ A P- well 132 may comprise P- semiconductor material of an integrated circuit substrate (not shown). The ESD structure ~~of the invention~~ may also be formed within a P- well located in an N- ~~substrate~~ semiconductor material of an integrated circuit substrate (not shown). An outer portion of the N+ diffusion 128a, the portion overlapping the N- well 130, is within the P- well 132. Another N+ diffusion 128b encircles the N+ diffusion 128a that ties together the N+ diffusions 128. The

another N+ diffusion 128b is in the P- well 132 and a field oxide 122 may be located between the N+ diffusion 128a and the another N+ diffusion 128b. In addition, the N+ diffusions 128 may be connected together by conductive vias connected together by conductive paths (not shown).